

P2083-B01

GK110, 3GB GDDR5, 384b, 64Mx32 +128Mx32
DVI_I+DVI_D + HDMI + DP

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	MEMORY: GPU Partition A/B
5	MEMORY: FBA[31:0]
6	MEMORY: FBA[63:32]
7	MEMORY: FBB[31:0]
8	MEMORY: FBB[63:32]
9	MEMORY: GPU Partition C/D
10	MEMORY: FBC[31:0]
11	MEMORY: FBC[63:32]
12	MEMORY: FBD[31:0]
13	MEMORY: FBD[63:32]
14	MEMORY: GPU Partition E/F
15	MEMORY: FBE[31:0]
16	MEMORY: FBE[63:32]
17	MEMORY: FBF[31:0]
18	MEMORY: FBF[63:32]
19	GPU PWR and GND
20	GPU Decoupling
21	DACA Interface
22	IFPAB DVI-I-DL
23	IFPEF DVI-D-DL
24	IFPC HDMI IFPC
25	IFPD DP

Page	Description
26	MIOA/B and Framelock Interface
27	MISC1: Fan, Thermal, JTAG, GPIO
28	MISC2: ROM, XTAL, Straps
29	PS: 5V, PEX_VDD
30	PS: FBVDD/Q
31	PS: NVVDD Controller
32	PS: NVVDD Phase 1,2
33	PS: NVVDD Phase 3,4
34	PS: NVVDD Phase 5,6
35	Power Connector Hot Unplug Detect
36	PS: Inputs, Filtering, and Monitoring
37	PS: Shutdown
38	PS: 12V Current Steering
39	MECH: Bracket/Thermal
40	POWER BRAKE AND LED

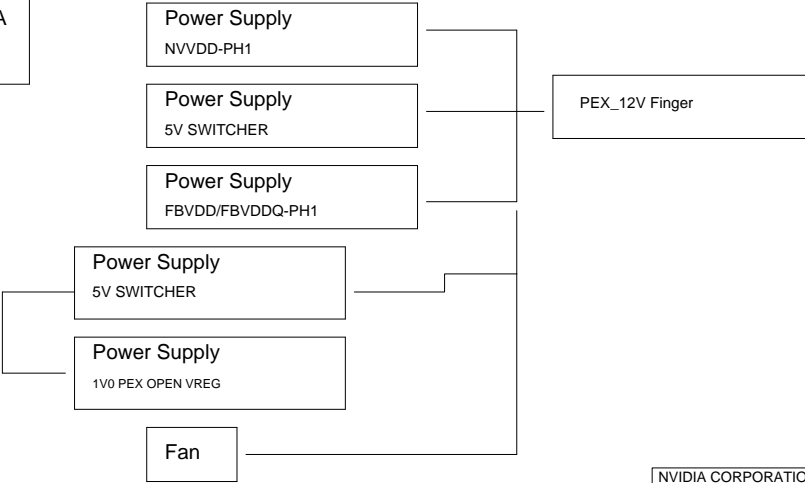
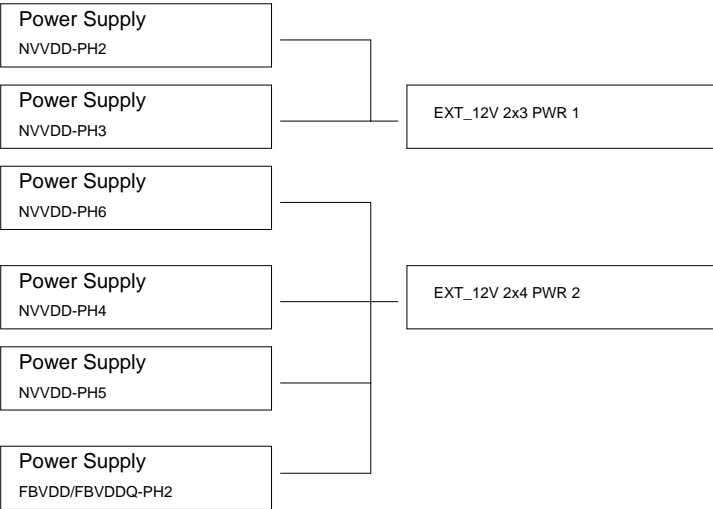
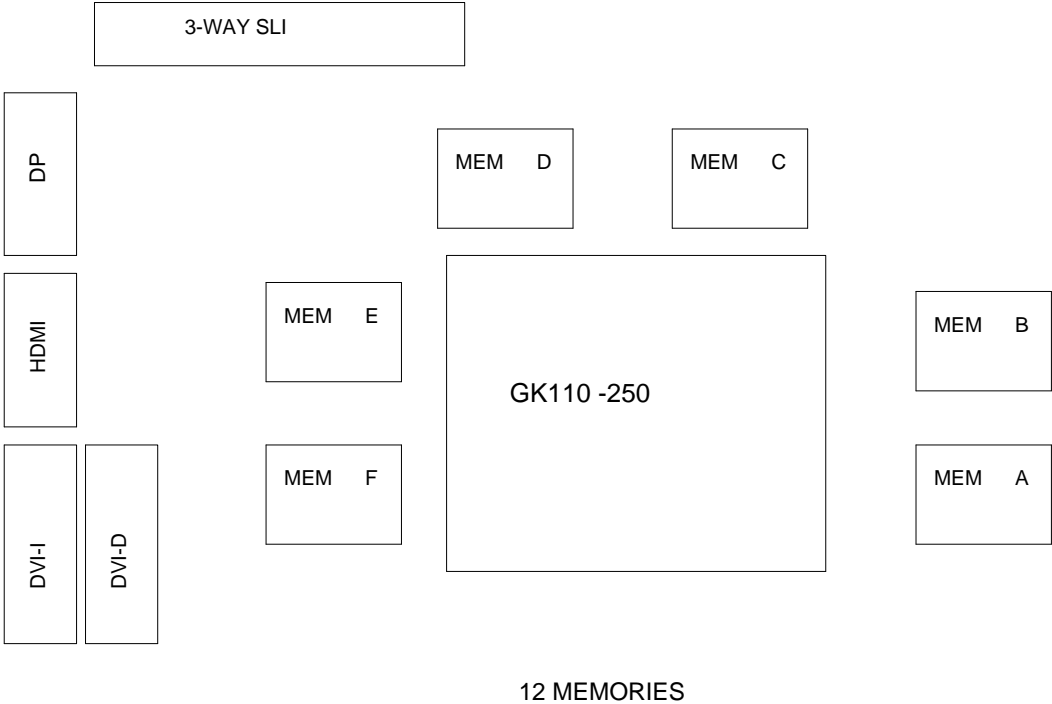
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Table of Contents

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
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NV_PN	600-12083-BASE-600		
PCB REV	P2083-B01	PAGE	1 OF 40
BOM REV	A	DATE	01-MAR-2013



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DESKTOP SKU SKU 0020

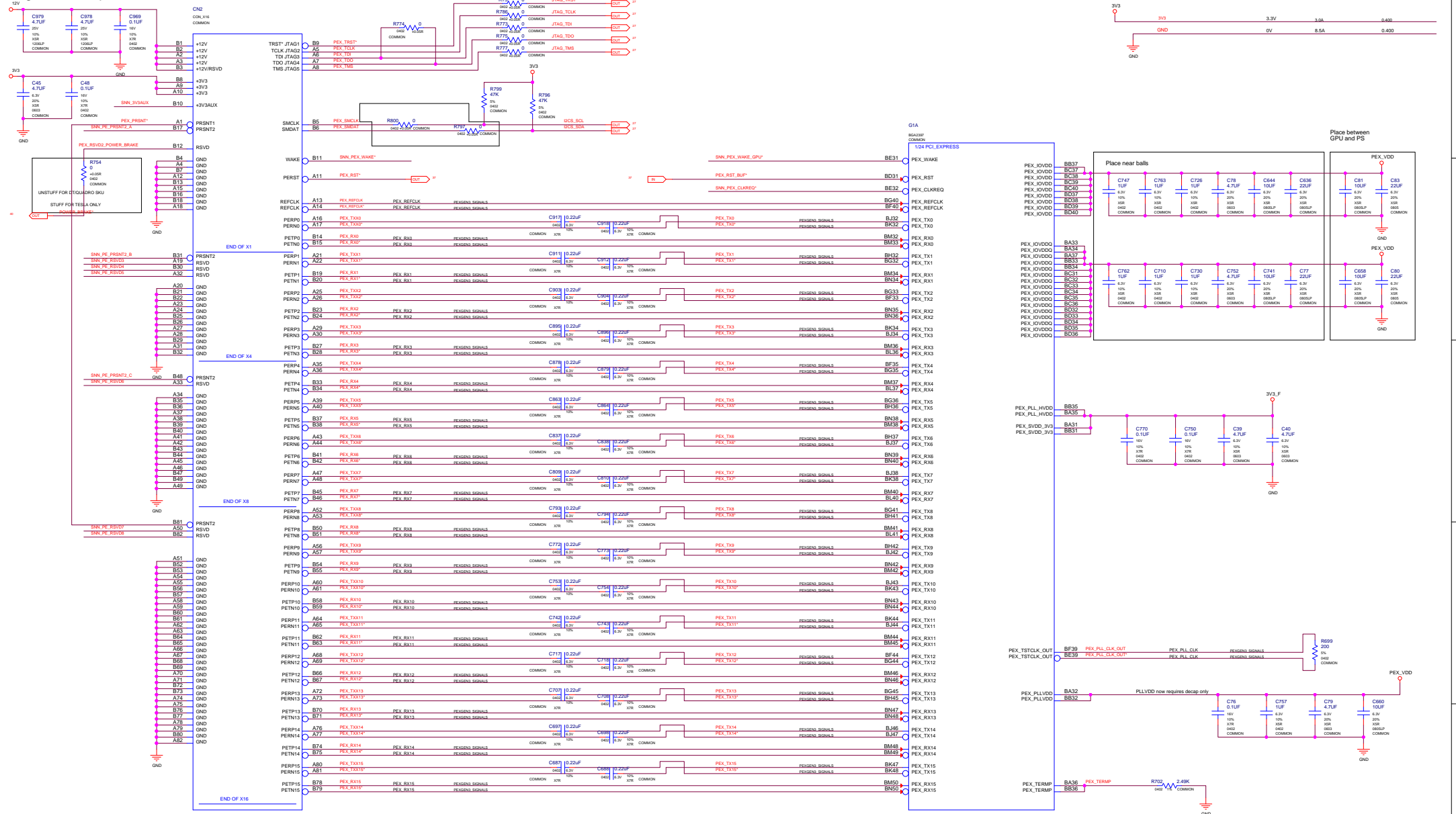


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Block Diagram

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-12083-BASE-600	PAGE	2 OF 40
PCB REV	P2083-B01	DATE	01-MAR-2013
BOM REV	A		

Page3: PCI Express



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PCI Express

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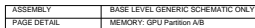
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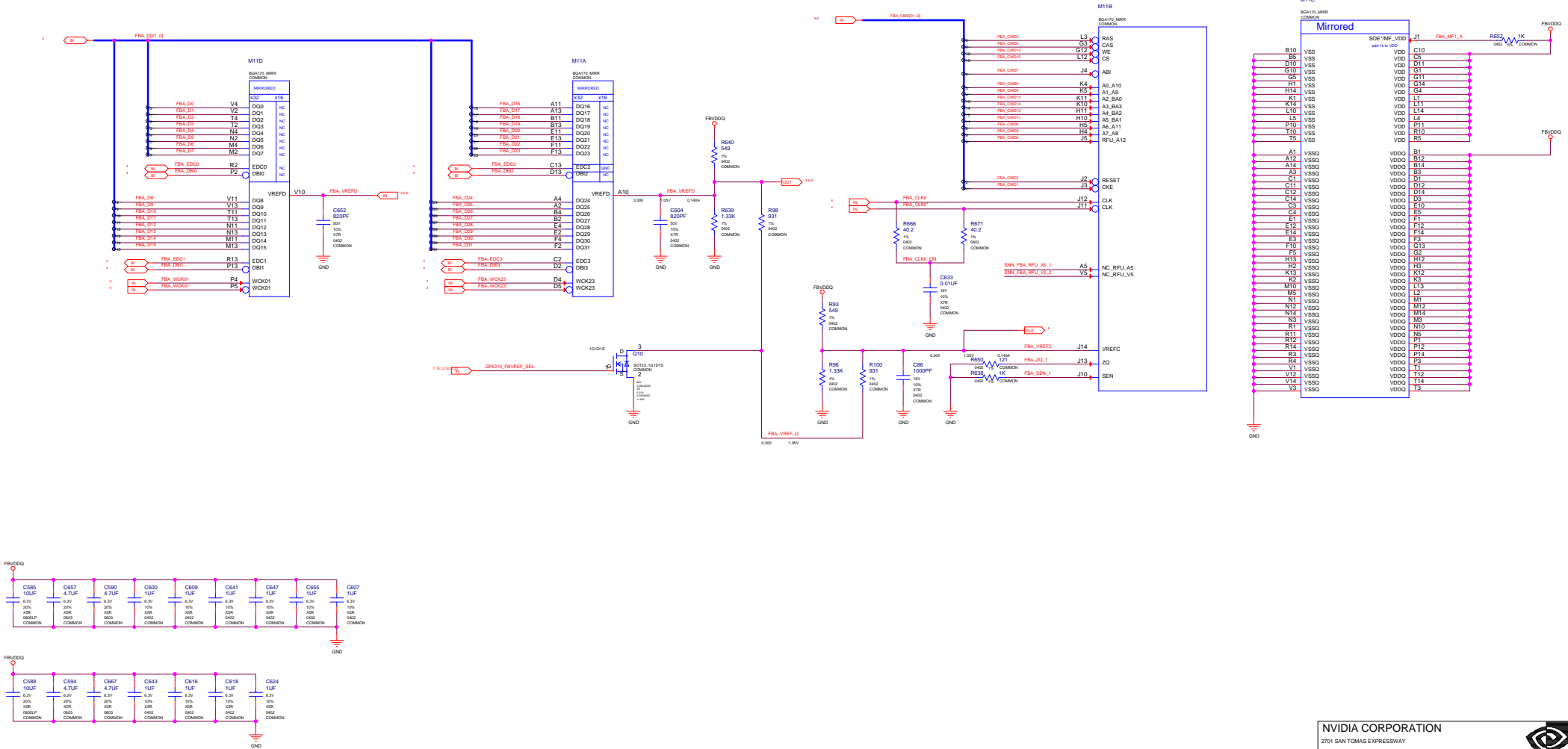
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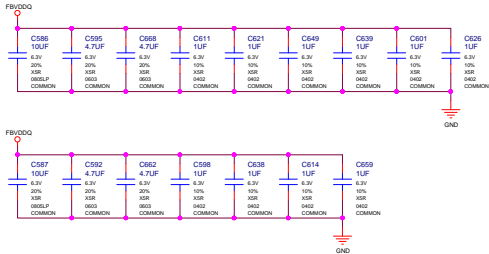





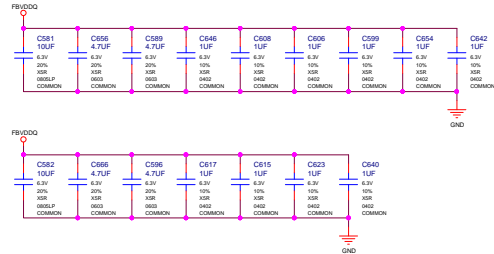
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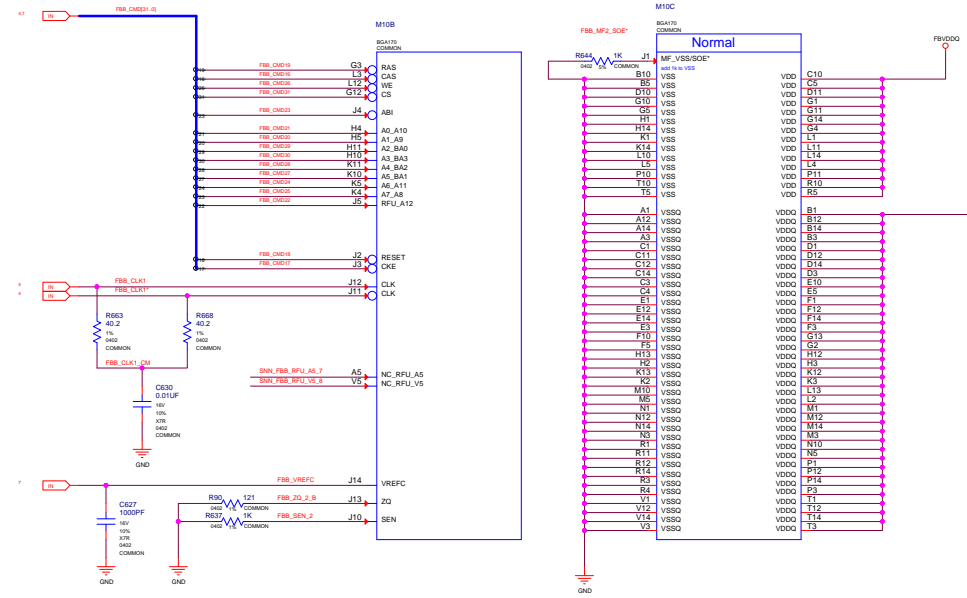
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SANTA CLARA, CA 95050, USA	
INV_P/N	600-12083-BASE-600
PCB REV	P2083-B01
BCM REV	A
PAGE	5 OF 40
DATE	01-MAR-2013




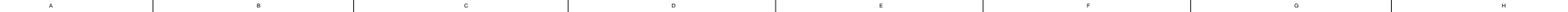
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PCB REV	P2083-B01	PAGE	6 OF 40
BOM REV	A	DATE	01-MAR-2013

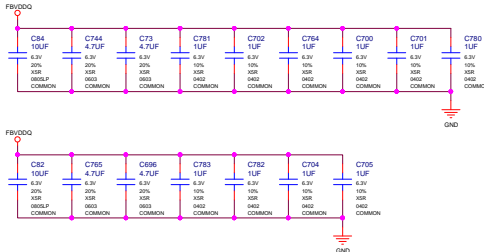


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NV_PN	600-12083-BASE-600		
PCB REV	P2083-B01	PAGE	7 OF 40
BOM REV	A	DATE	01-MAR-2013



NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-12083-BASE-600		
PCB REV	P2083-B01	PAGE	8 OF 40	
BOM REV	A	DATE	01-MAR-2013	





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PAGE DETAIL	MEMORY: FBC(31:0)

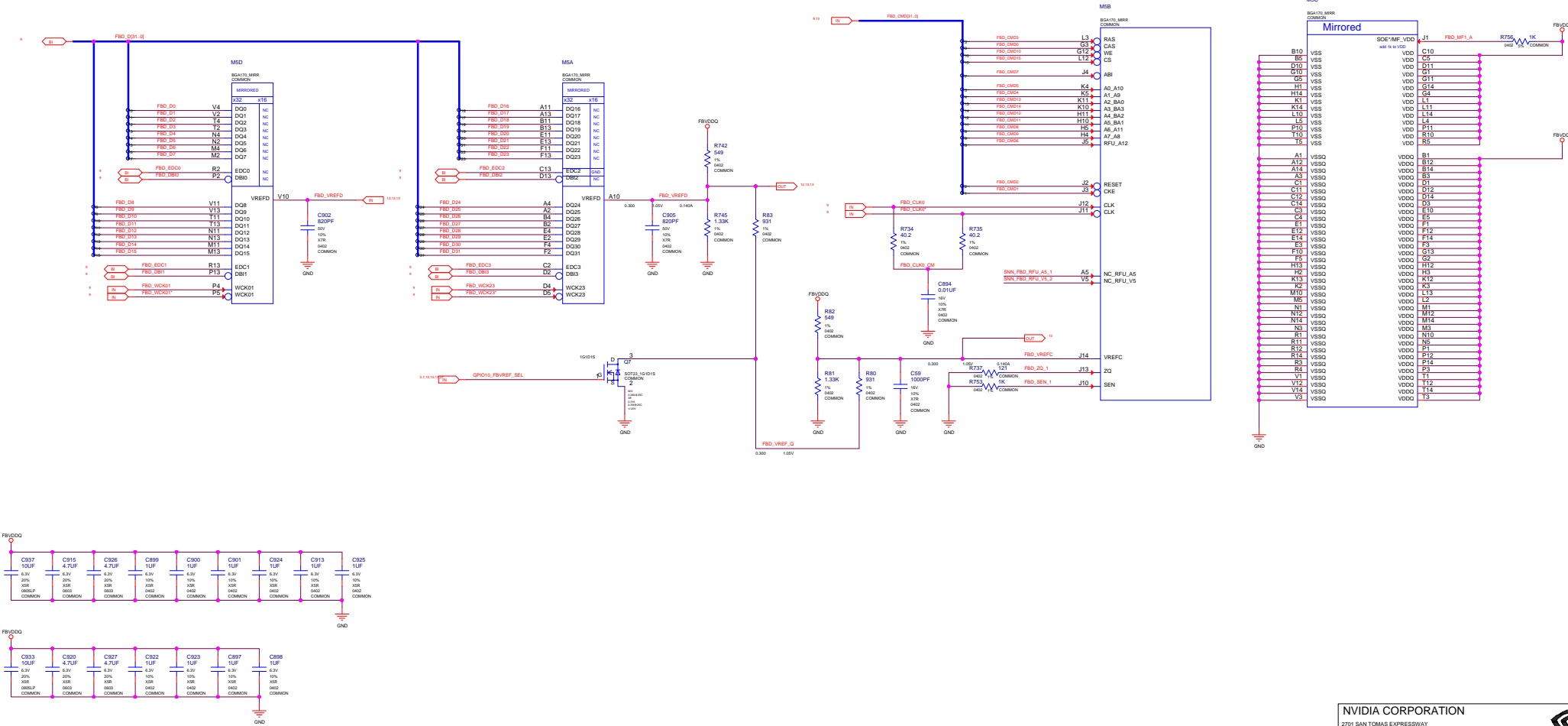
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PCB REV	P2083-B01
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BOM REV	A
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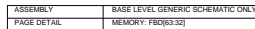
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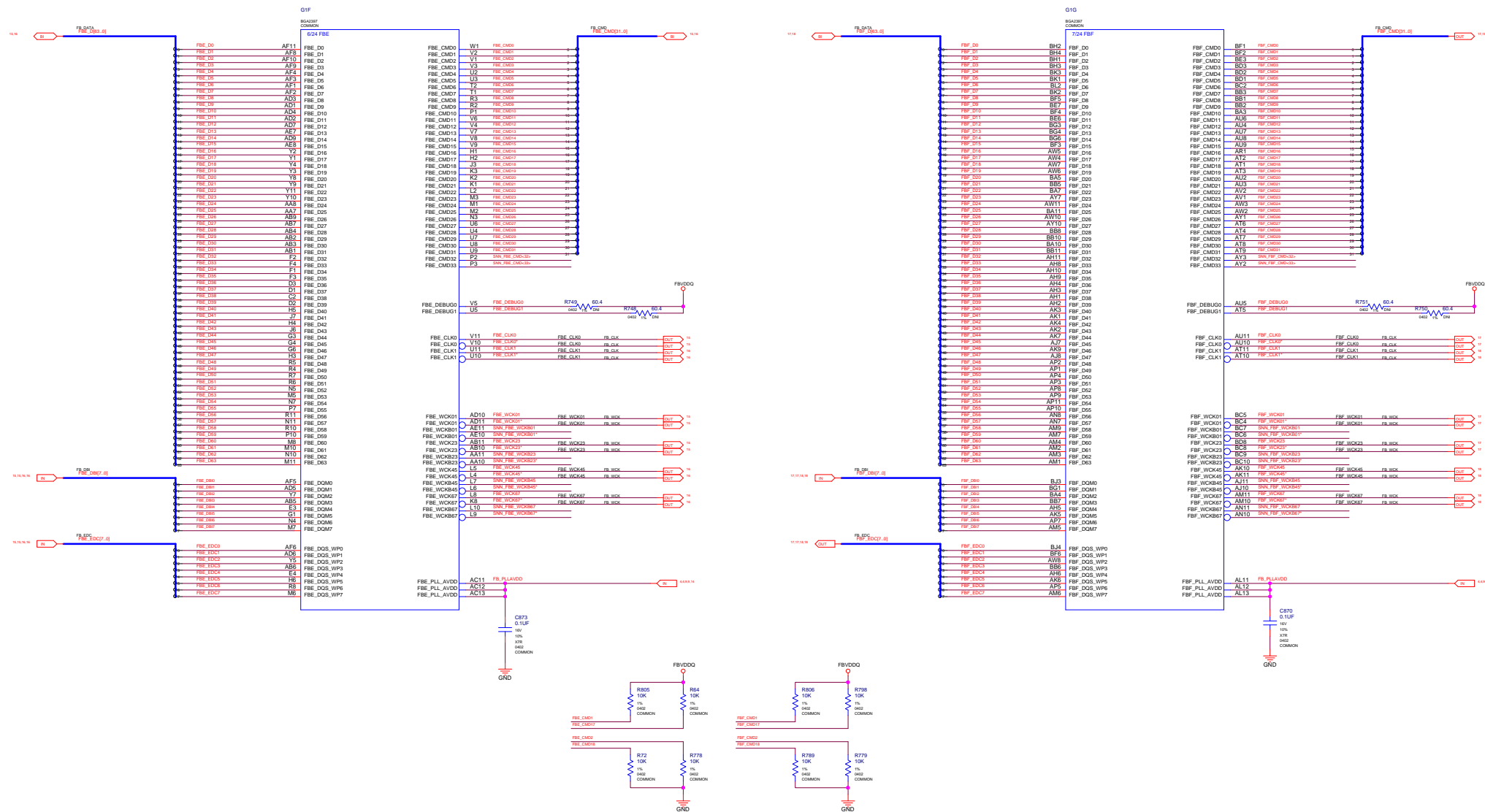
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SANTA CLARA, CA 95050, USA	
INV_PN	600-12083-BASE-600
PCB REV	P2083-B01
BOX REV	A
PAGE	12 OF 40
DATE	01-MAR-2013



BOM REV	A	DATE	01-MAR-2013
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BOM REV	A	DATE	01-MAR-2013
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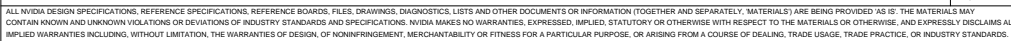



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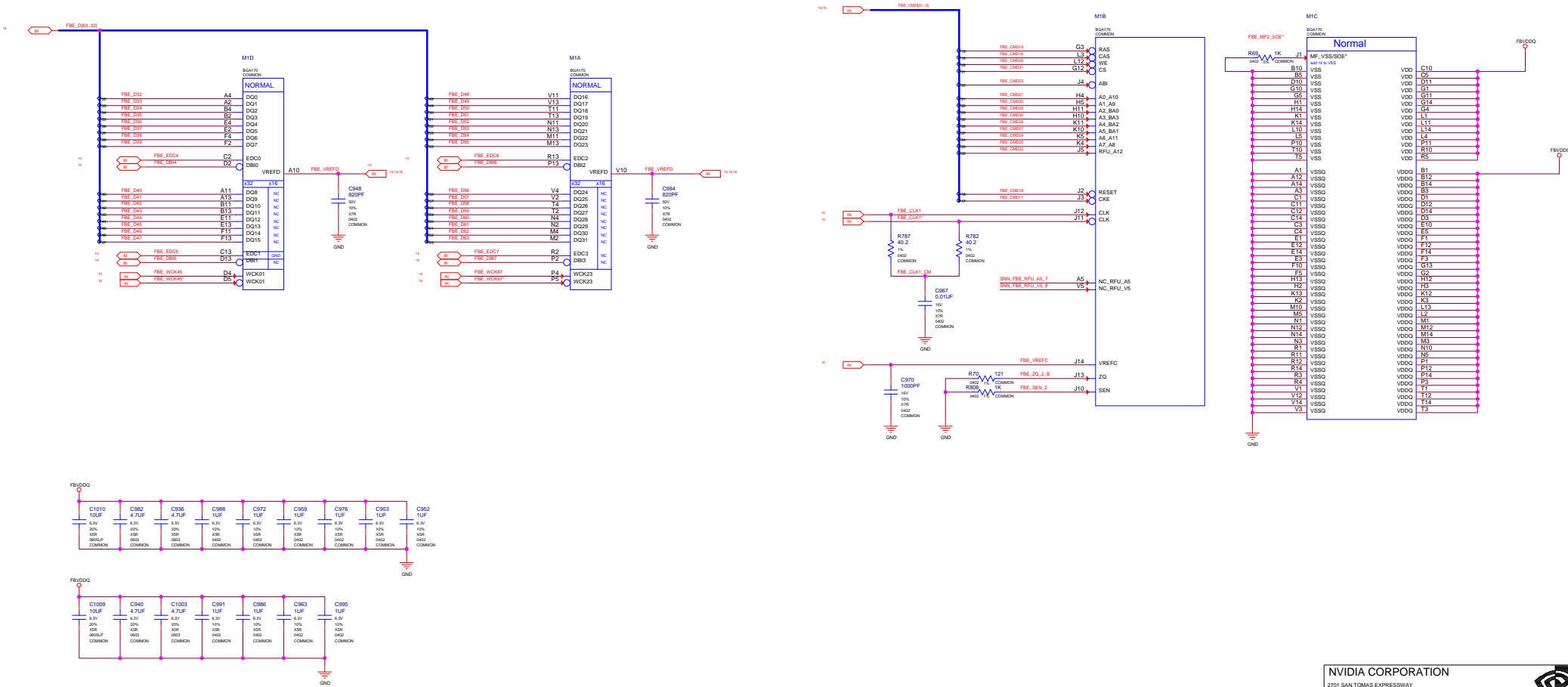
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NV_PN 600-12083-BASE-600

PCB REV P2083-B01 PAGE 14 OF 40
BOM REV A DATE 01-MAR-2013



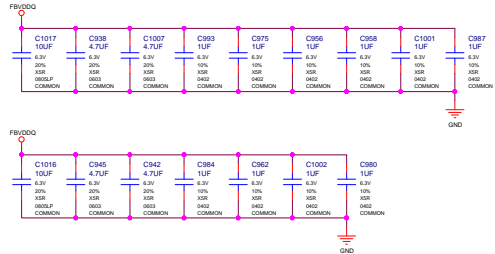
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN	600-12083-BASE-600		
PCB REV	2083-B01	PAGE	15 OF 40
BOM REV	A	DATE	01-MAR-2013




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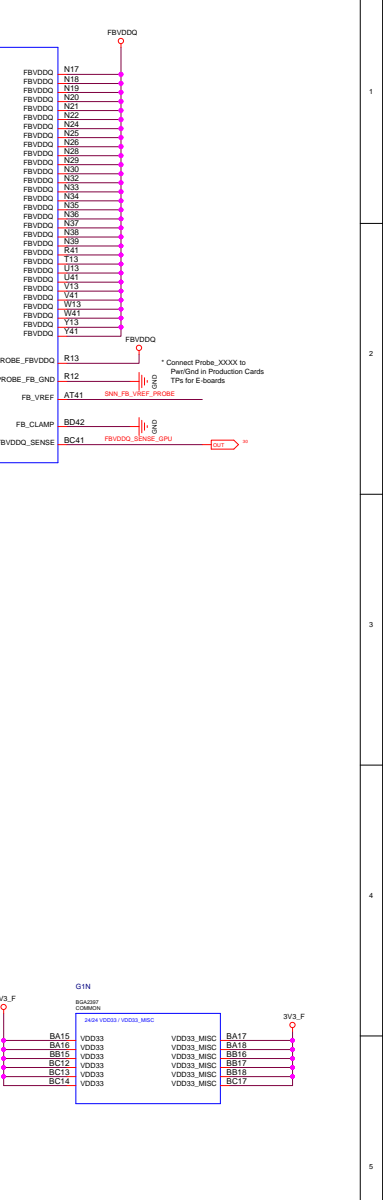
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PAGE DETAIL	MEMORY: FBE(63..32)

NVIDIA CORPORATION	
2701 SAN TOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
INV_PN	600-12083-BASE-600
PCB REV	P2083-B01
BOX REV	A
PAGE	16 OF 40
DATE	01-MAR-2013

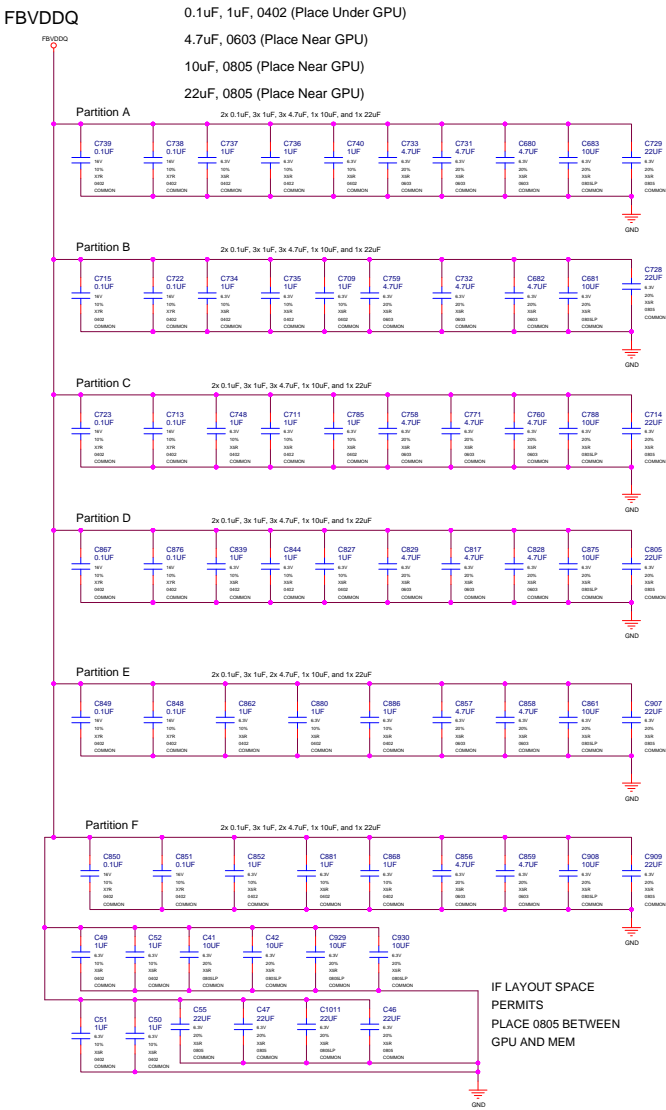


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NV_PN	600-12083-BASE-600		
PCB REV	P2083-B01	PAGE	17 OF 40
BOM REV	A	DATE	01-MAR-2013

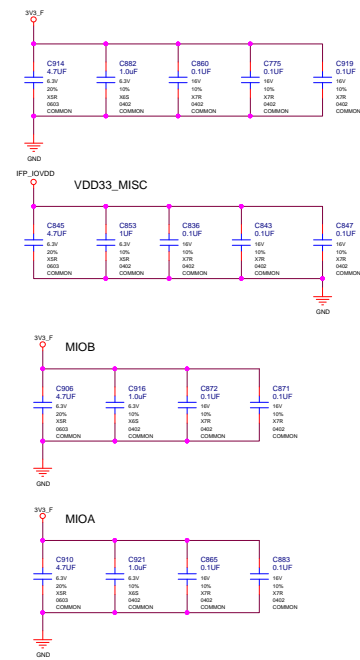
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Based on GB3-X GDDR5 FBVDDQ Decap Guideline

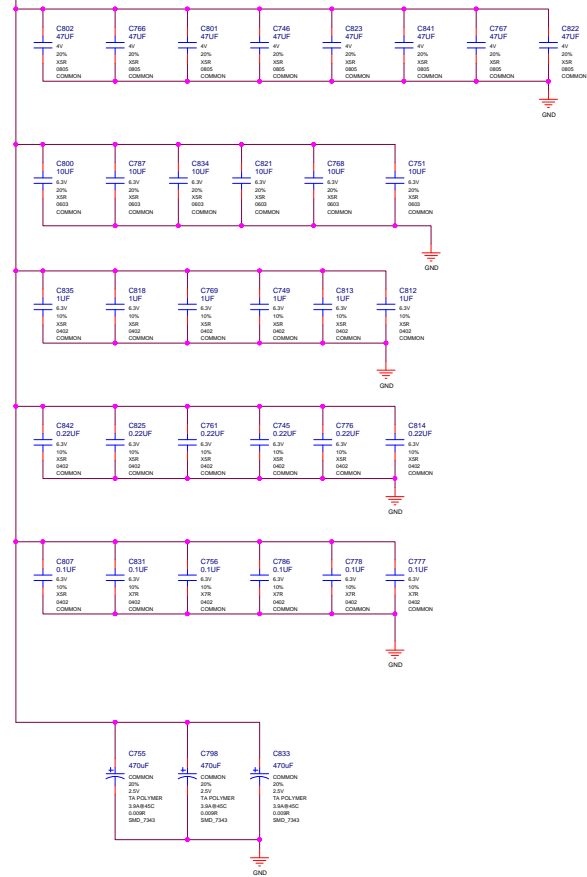


VDD33



NVVDD Decoupling caps. Place under GPU.

NVVDD



8x 47uF, 0805

6x 10uF, 0603

4x 1uF, 0402

4x 0.22uF, 0402

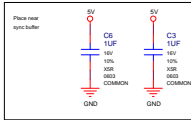
4x 0.1uF, 0402


3x 330uF, SMD7343

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PAGE DETAIL	GPU Decoupling


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2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
INV_PN	600-12083-BASE-600	PAGE	20 OF 40
PCB REV	P2083-B01	DATE	01-MAR-2013
BCM REV	A		

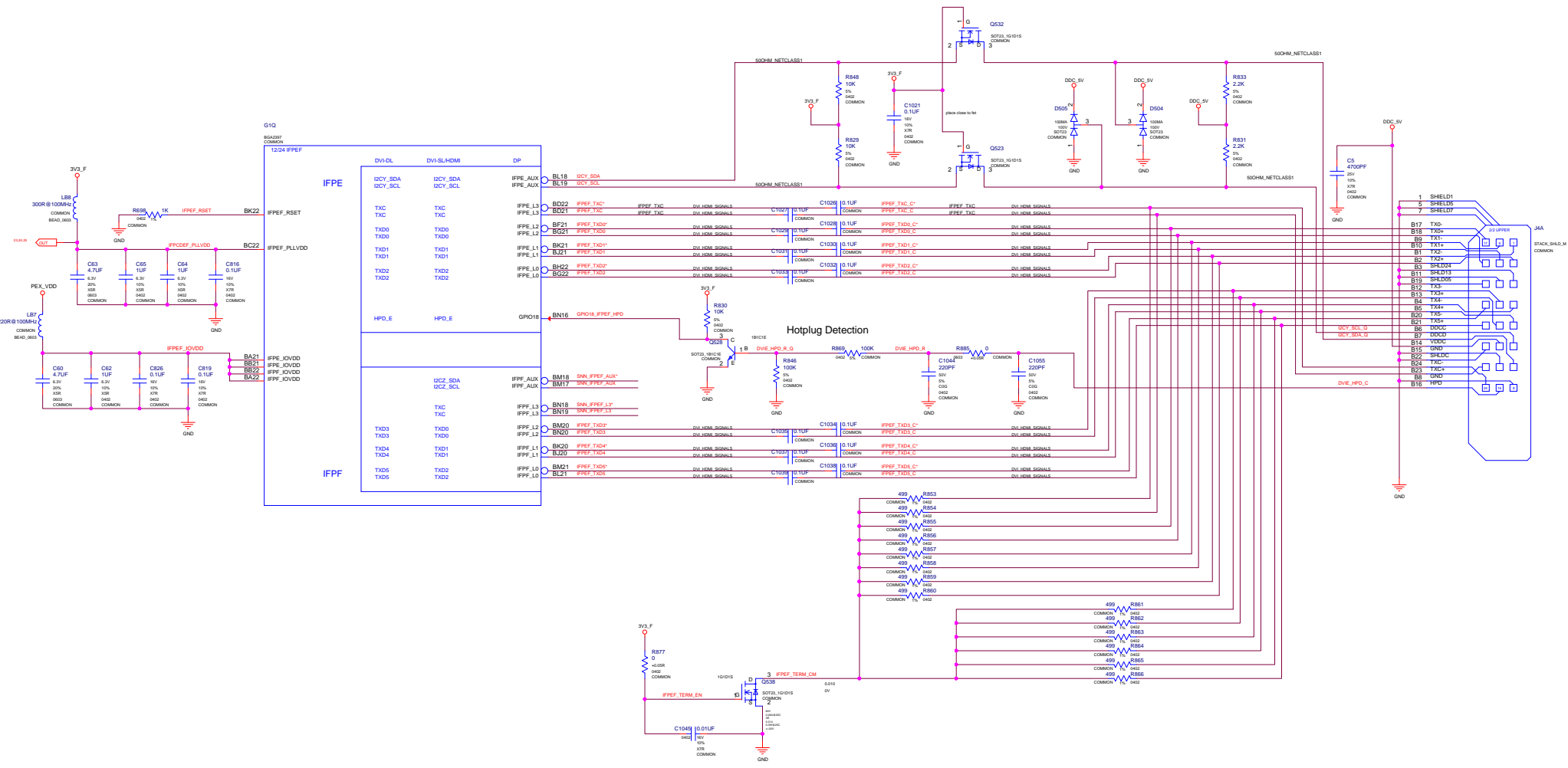



NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN	600-12083-BASE-600		
PCB REV	P2083-B01	PAGE	21 OF 40
BOM REV	A	DATE	01-MAR-2013



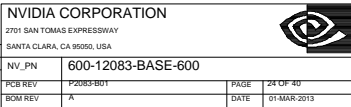


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NV_PN		600-12083-BASE-600	
PCB REV	P2083-B01	PAGE	22 OF 40
BOM REV	A	DATE	01-MAR-2013

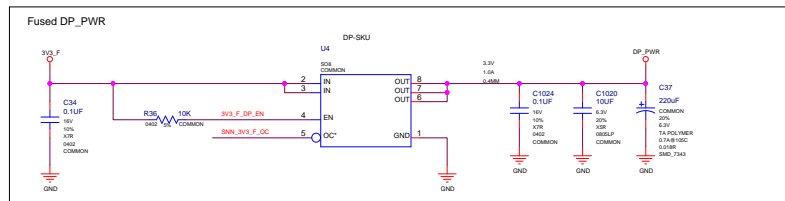
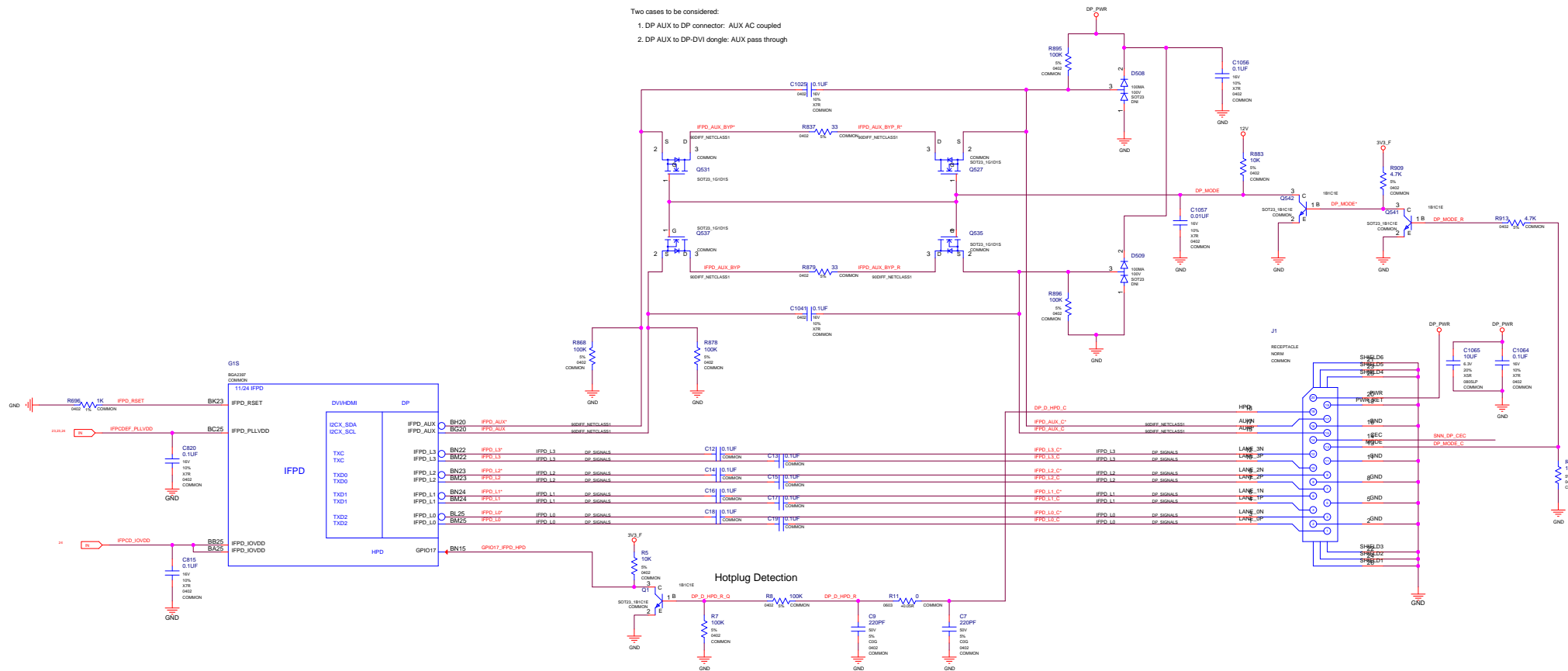


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NV_PN 600-12083-BASE-600			
PCB REV P2083-B01	PAGE 23 OF 40		
ROM REV A	DATE 01-MAR-2013		


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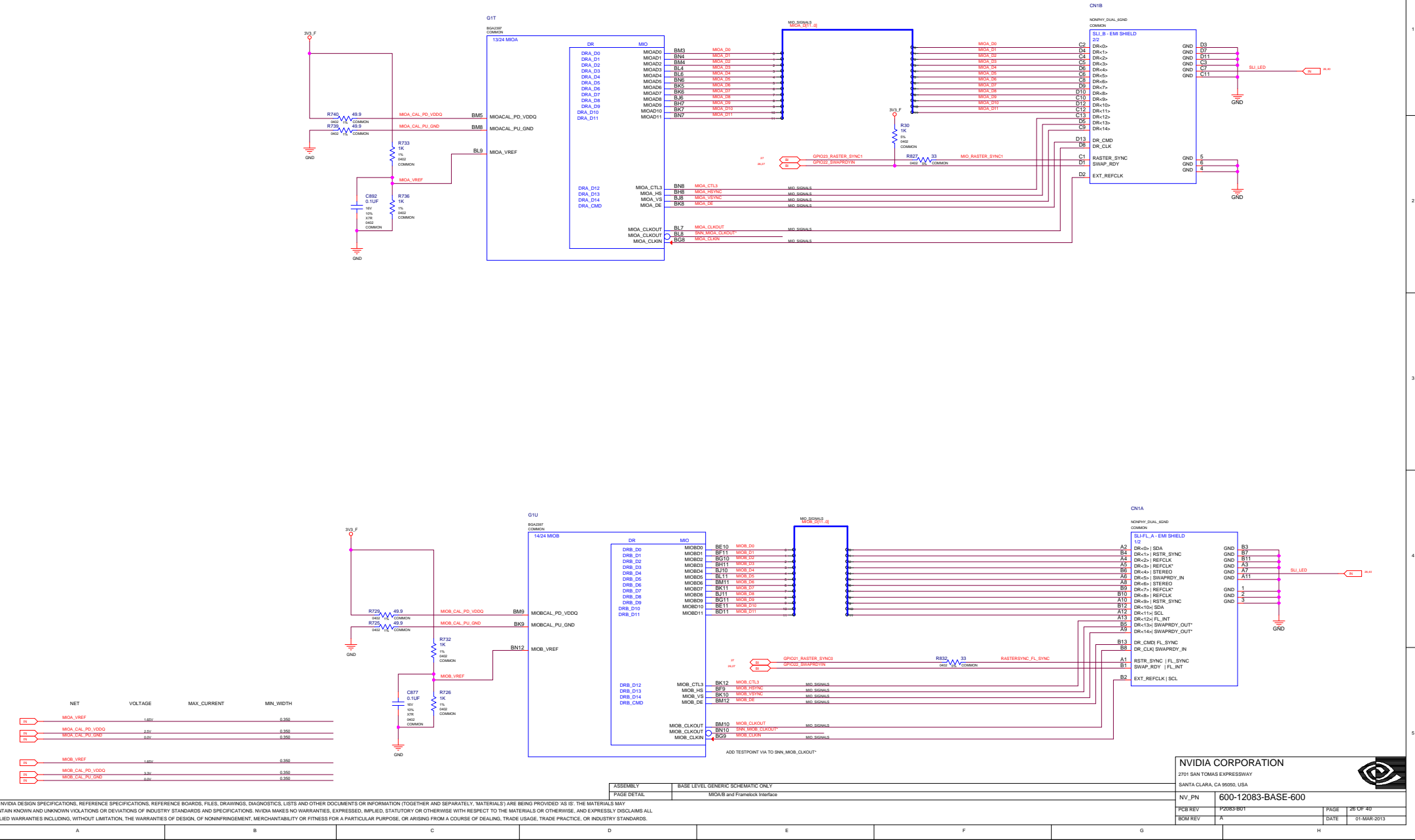
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2. DP AUX to DP-DVI dongle: AUX pass through

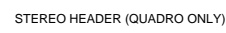


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PAGE DETAIL	IFPD DP

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN		600-12083-BASE-600	
PCB REV	P2083-B01	PAGE	25 OF 40
BOM REV	A	DATE	01-MAR-2013

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PACKAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO



A	B	C	D	E	F	G	H
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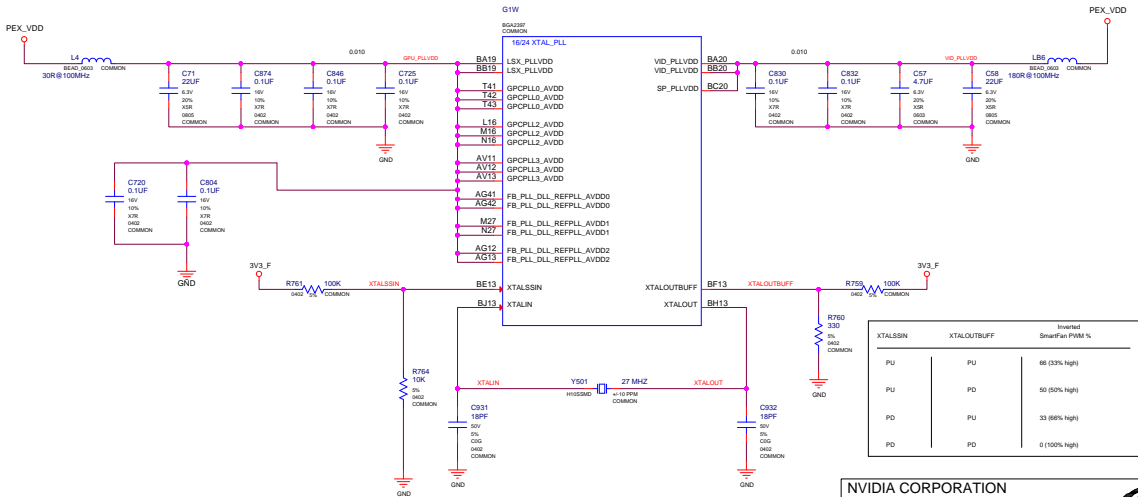
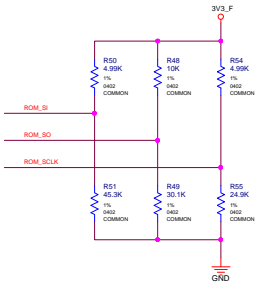
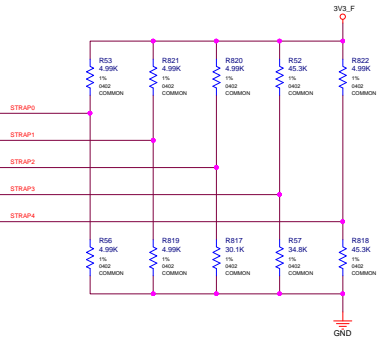
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STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0100* (DEVID :0x1004)	25K PD -300 GPU PCI DEV ID 0x1004
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	
	RAMCFG[2]*	1*	
	RAMCFG[3]*	0*	
	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	
	FB[0]_APERTURE_SIZE*	1* For 128MB*	
	FB[1]_APERTURE_SIZE*	0* For 128MB*	
	PEX_PLL_ENL_TERM100*	0* DISABLED*	
	PCI_DEVID_EXT[5]*	0*	
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0*	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

x32 DENSITY MODE STRAPS		
CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 384-bit Elpida	
0010	32Mx32 384-bit Hynix	
0011	32Mx32 384-bit Samsung	
0100	Reserved	
0101	64Mx32 384-bit Elpida	
0110	64Mx32 384-bit Hynix	
0111	64Mx32 384-bit Samsung	
1000	Reserved	
1001	32Mx32 320-bit Elpida	
1010	32Mx32 320-bit Hynix	
1011	32Mx32 320-bit Samsung	
1100	Reserved	
1101	64Mx32 320-bit Elpida	
1110	64Mx32 320-bit Hynix	
1111	64Mx32 320-bit Samsung	

x16 DENSITY MODE STRAPS		
CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	64Mx16 384-bit Elpida	
0010	64Mx16 384-bit Hynix	
0011	64Mx16 384-bit Samsung	
0100	Reserved	
0101	128Mx16 384-bit Elpida	
0110	128Mx16 384-bit Hynix	
0111	128Mx16 384-bit Samsung	
1000	Reserved	
1001	64Mx16 320-bit Elpida	
1010	64Mx16 320-bit Hynix	
1011	64Mx16 320-bit Samsung	
1100	Reserved	
1101	128Mx16 320-bit Elpida	
1110	128Mx16 320-bit Hynix	
1111	128Mx16 320-bit Samsung	

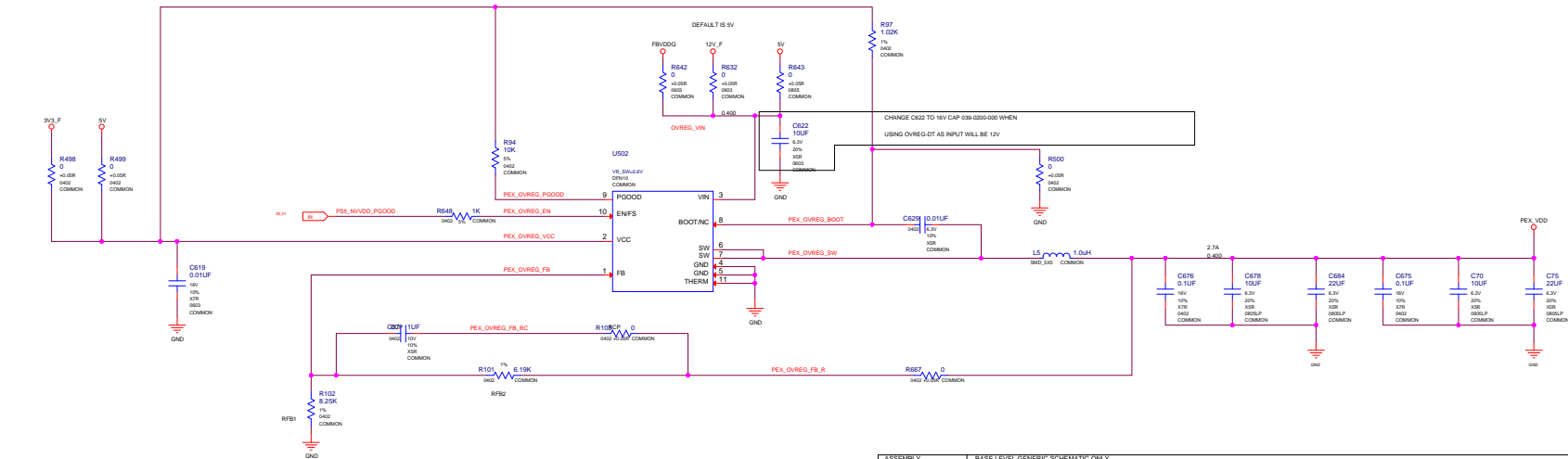
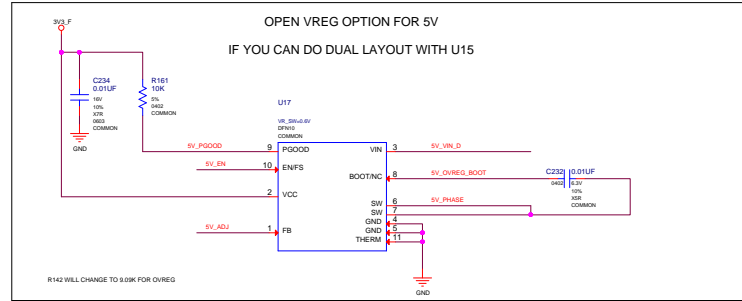
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BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	45.3K 1% TO GND




XTALSSIN			XTALOUTBUFF			Inverted SmartFan PWM %		
PU		PU						66 (33% High)
PU		PD						50 (50% High)
PD		PU						33 (86% High)
PD		PD						0 (100% High)

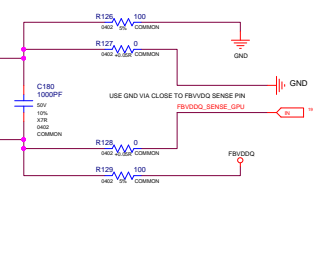
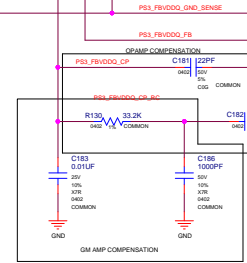
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INV_PN	600-12083-BASE-600		
PCB REV	P2083-B01	PAGE	28 OF 40
BIOM REV	A	DATE	01-MAR-2013


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 5V, PEX_VDD

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NV_PN	600-12083-BASE-600		
PCB REV	P2083-B01	PAGE	29 OF 40
BOM REV	A	DATE	01-MAR-2013

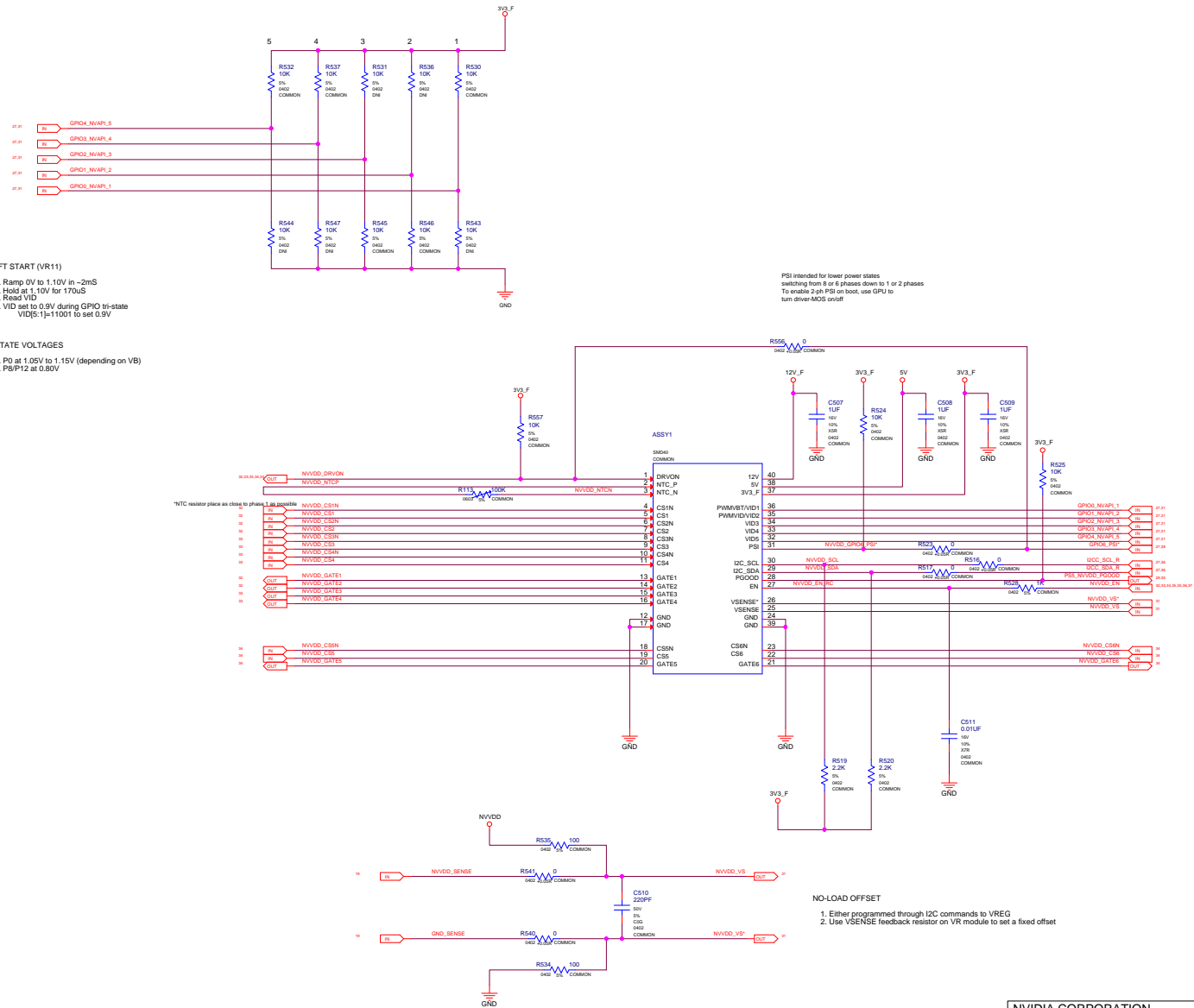


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NV_PN		600-12083-BASE-600	
PCB REV	P2083-B01	PAGE	30 OF 40
BOM REV	A	DATE	01-MAR-2013



VID Table

GPIO4 VID_5	GPIO3 VID_4	GPIO2 VID_3	GPIO1 VID_2	GPIO0 VID_1	VOUT
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

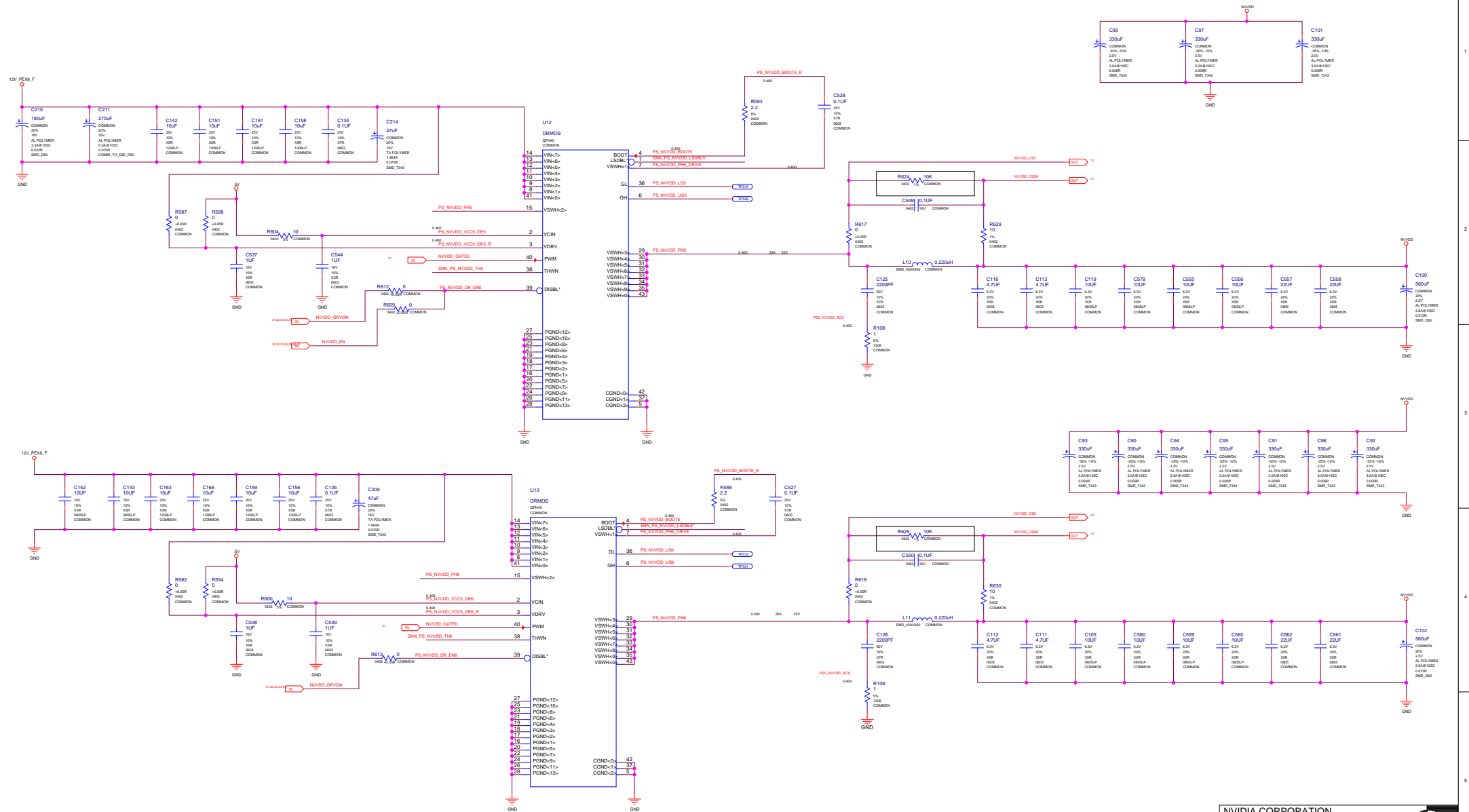


1. Either programmed through I2C commands to VREG
2. Use VSENSE feedback resistor on VR module to set a fixed offset



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NV_PN	600-12083-BASE-600		
PCB REV	P2083-B01	PAGE	32 OF 40
BOM REV	A	DATE	01-MAR-2013



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ASSEMBLY
PAGE DETAIL

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PS: NVVDD Phase 5,6

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P2083-B01

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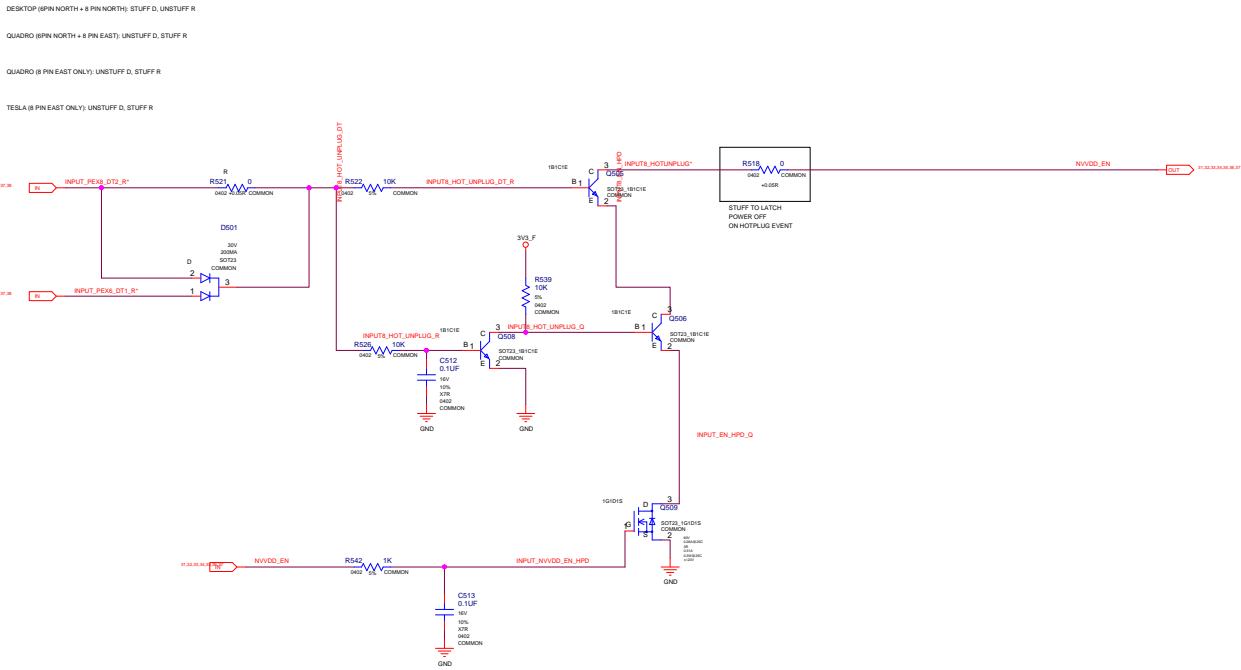
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PAGE

34 OF 40

DATE

01-MAR-2013



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P2083-B01

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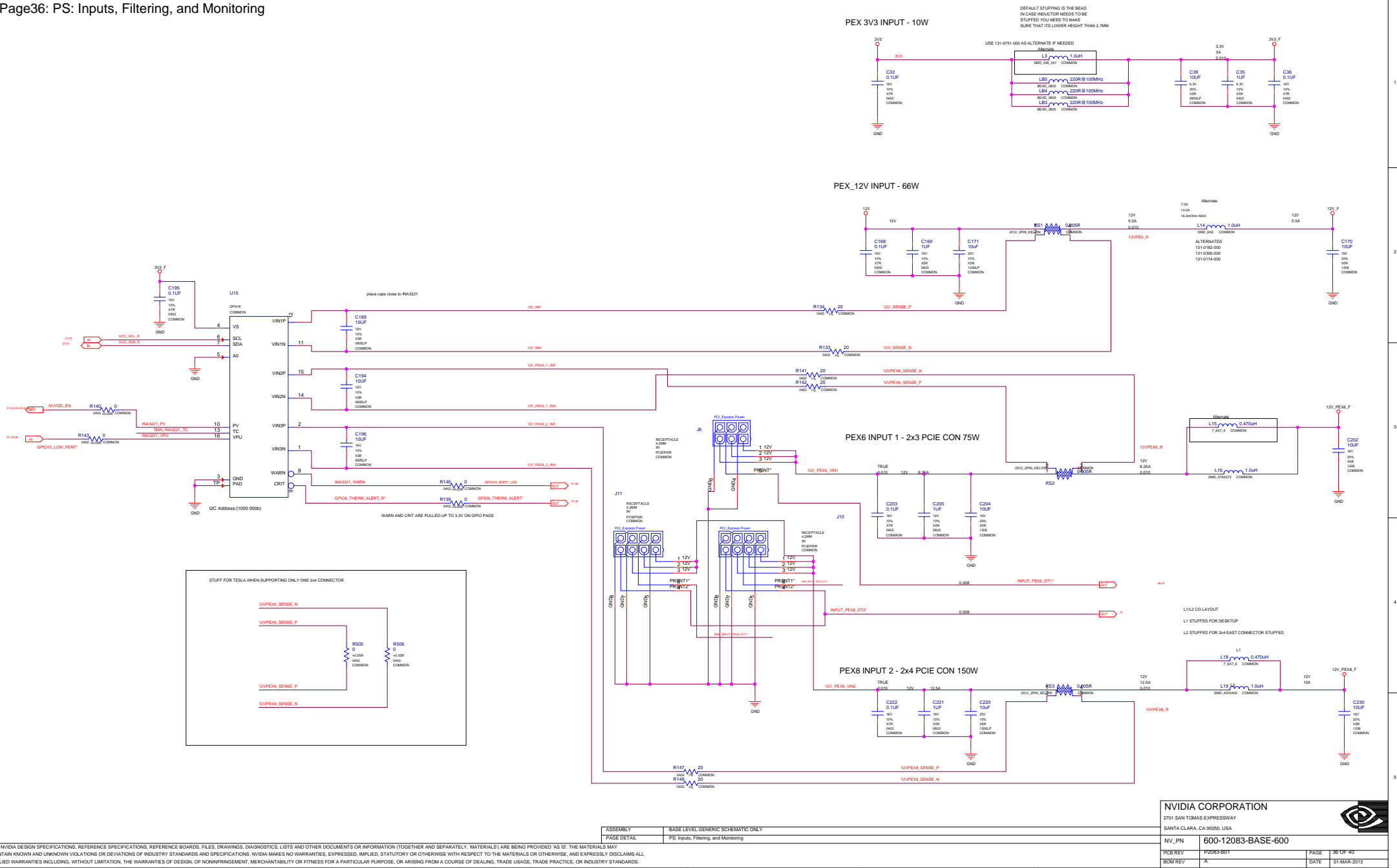
PAGE

35 OF 40

DATE

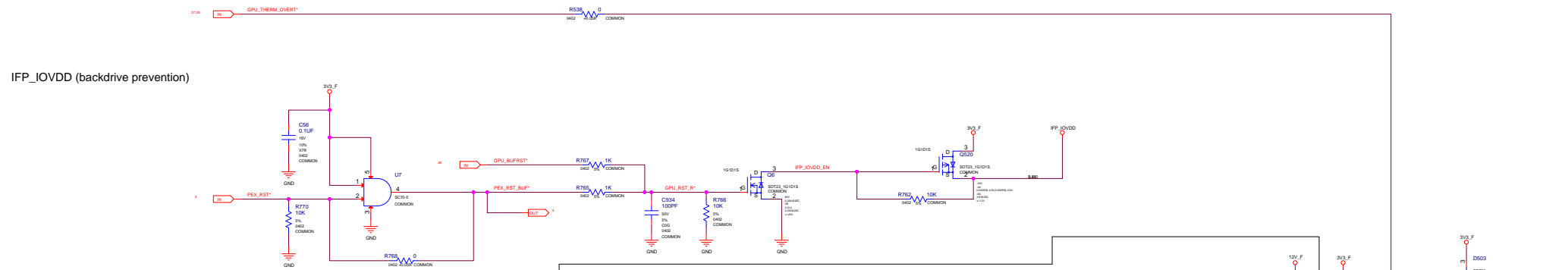
01-MAR-2013



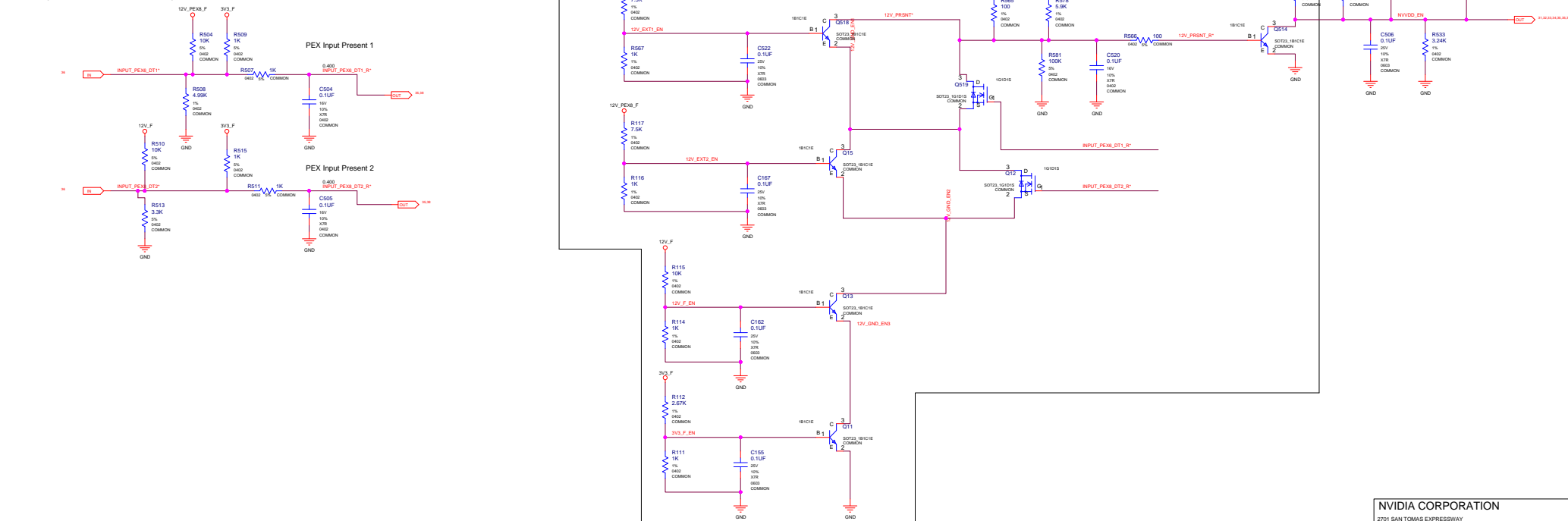


THERM OVERT SHUTDOWN

IFP_IOVDD (backdrive prevention)



PEX Input - NVVDD Power Sequence



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Shutdown

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NV_PN	600-12083-BASE-600
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PCB REV	P2083-B01	PAGE	37 OF 40
BOM REV	A	DATE	01-MAR-2013

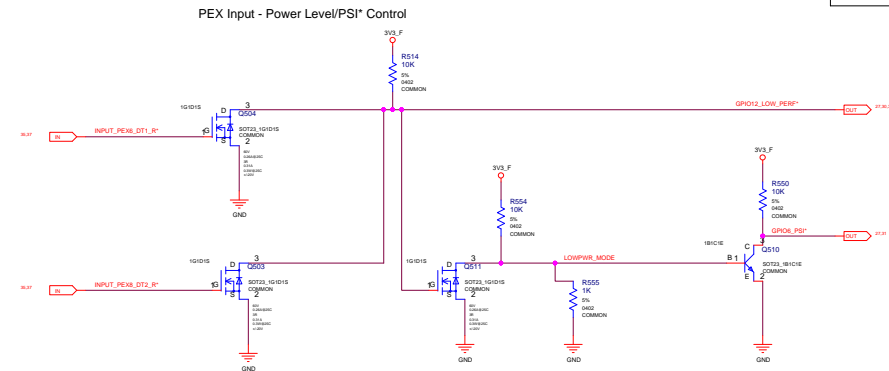
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GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

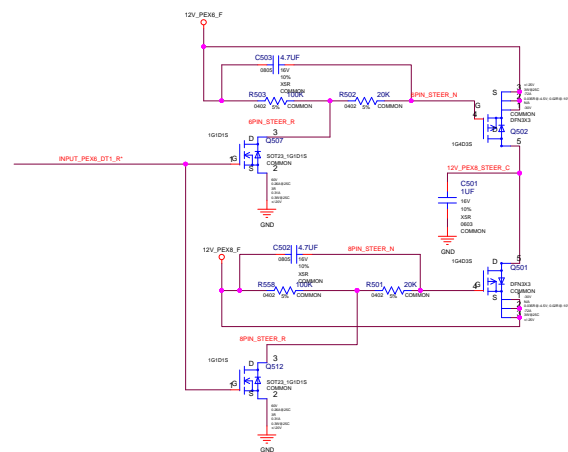
DT SKU + WS SKU:
FULL POWER WHEN BOTH 6PIN+8PIN ARE PRESENT
STUFF Q508 AND Q509

TESLA SKU:
FULL POWER WHEN 6PIN+8PIN OR 8PIN ONLY ARE PRESENT
STUFF Q508 ONLY



12V Current Steering FETs FROM 8PIN TO 6PIN (TESLA ONLY)

STUFF FOR TESLA ONLY



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 12V Current Steering

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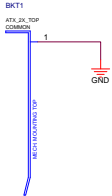


NV_PN	600-12083-BASE-600		
PCB REV	P2083-B01	PAGE	38 OF 40
BOM REV	A	DATE	01-MAR-2013

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Brackets:

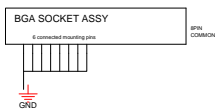
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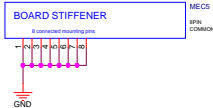
Bracket Screw



GPU SOCKET



GPU Stiffener (BRING-UP COOLER)



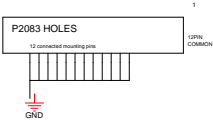
Hockey Stick



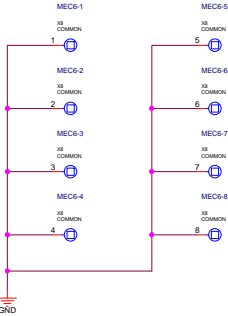
Stiffener



Mechanical Holes Symbol



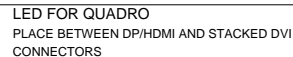
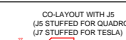
Bring Up Cooler




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PAGE DETAIL	MECH: Bracket/Thermal

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NV_PN	600-12083-BASE-600	PAGE	39 OF 40
PCB REV	P2083-B01	DATE	01-MAR-2013
BOX REV	A		



NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN		600-12083-BASE-600	
PCB REV	P2083-B01	PAGE	40 OF 40
BOM REV	A	DATE	01-MAR-2013



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